Communication

APPLICATIONS OF NANOELECTRONICS AND NANO-MAGNETICS

B.Naresh

S.V.R.K.Govt. Degree College, Nidadavole, AP, India

There have been many significant advances in nanoelectronic materials and devices during the first decade of the 21st Century, but nowhere has the impact of shrinking devices to the nanoscale been more dramatic than in the semiconductor industry. For over 30 years, the industry has been able to double the number of field-effect transistors (FETs) on a chip every 18–24 months, a trend that has come to be known as “Moore’s Law”. The resulting exponential increase in the information-processing capability per unit area on the chip or more importantly, per dollar has meant not only that existing chip-based products have become faster and/or cheaper each year, but also that the number of products that use semiconductor chips has greatly expanded, from supercomputers to cell phones to toasters. The result can clearly be seen in the exponential increase in semiconductor revenues as the transistor size has shrunk .Over the past decade, the industry has nearly doubled in size, and is expected to hit a record high of $300B in 2010, with the U.S. market share being approximately 50% of that. It is a driver of most economies of the developed world.

These advances have been won with increasing difficulty in recent years, and continuing them will require ever increasing utilization of nanoscale structures and properties. According to the long-established rules for transistor scaling, the operating voltage should be reduced in proportion to the reduction in the critical dimensions of the FET. Following this prescription, the speed of the FET went up while the area occupied by the device and power used by the device went down, so that the areal power density remained constant. In the past 10 years, as devices shrank below 100 nm in gate length, the rule governing reduction of voltage had to be abandoned, primarily because a minimum gate voltage swing is necessary to switch an FET from an “off” (low-current) state to an “on” (high current) state. If that swing is too small, the device will have excessive leakage current (high passive power dissipation) in the nominally “off” state or low current (slow circuits) in the nominally “on” state. While it seems that devices can continue to be shrunk for the next 5–10 years, the designs utilizing them must increasingly trade density for speed in order to mitigate the increasing on-chip power density. This will in limit the ability of further size reduction to achieve the full historical benefits of increasing computation/second/dollar/watt that has driven the industry up

Citation: Naresh B

Applications of nanoelectronics and nanomagnetics, J.Adv.Sci.Eng&Tech, 4,1,2024, 28

Received on 15th January 2024

Revised on 19th January 2024

Accepted on 28th January 2024

Copyright: © 2024 by the authors. Licensee AQIE and RIPS, KPHaveli, Khammam, Telangana, India. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY)license.

to now. Moreover, while the power-density challenge is affecting all applications (including large servers in datacenter environments), the overall energy consumption is even more problematic for the increasing number of mobile devices. These require not only finding a device with low operation energy, but also ultra-low (or zero) passive and standby energy needs. The trade-off between performance and leakage current is especially difficult in these applications and finding novel non-volatile devices potentially even for the logic devices would offer major advantages. In addition, finding ultra-low power transistors not only increases traditional battery life, but opens the door to more exotic energy scavenging techniques to power these devices in the future. In addition, as FETs have been shrunk to the tens of nanometers size range, rather than benefiting from new phenomena at the nanoscale, their performance has been challenged by increases in tunneling currents and the need for almost atomic-scale precision in fabrication. At the 90 nm node in the first part of the decade, for example, the gate insulator was approaching 1.5 nm in thickness just a few atomic layers of silicon oxy-nitride which not only resulted in unacceptably high tunneling leakage currents but also required monolayer control across a 200 mm wafer. The solution was to introduce an insulator with higher dielectric constant, which allowed for an increased thickness but in most cases also required changing the gate electrode process to a combination of poly silicon and metal. The result was decreased electrical thickness, which allowed further shrinking of the gate length. However, even with high-K material, the insulator thickness is still only a few nanometers, and with a lowered barrier height. Further improvements in gate dielectric materials will probably be limited, and therefore further reduction of gate length may depend on introduction of new device structures as discussed below. The gate length for modern transistors is now about 30 nm. This is exceedingly difficult to achieve with current optical lithography, which utilizes 193 nm wavelengths light to pattern the features. It is only possible through many tricks, including chemically active resists, restricted design rules, extensive use of optical proximity correction on the masks, and most recently, the introduction of immersion techniques to reduce the effective refractive index for the exposure. Moreover, since many of the electrical properties of the FET are exponentially dependent on gate length (including leakage currents), these dimensions must be controlled to just a few nanometers. Variations in line width across a wafer, and increasingly across a single die, are one of the major sources of variability that limit ultimate chip yield and performance, so it is crucial that new patterning solutions are found. The current approach for the industry is to push optical lithography to the extreme ultraviolet (EUV) range, but this continues to be a huge challenge, largely in finding suitable mask and resist materials, and significant research in this area is still required. Beyond optical lithography, emerging patterning processes such as nanoimprint lithography, scanning probe lithography, and various forms of self assembly are being explored. These are key areas of research for the coming decade. It is important to note that both the gate oxide and lithography improvements were only possible due to the research in nanoscale fabrication and characterization that has taken place over the past 10 years. Continued scaling will require further fundamental advances in lithographic and other processes for precise fabrication of nanometer-scale structures. Advances in metrology will be necessary to attain the required precision. Furthermore, future

 Copyright by AQIE and RIPS

devices must take direct advantage of nanoscale effects as well. One interesting example that has already reached the market is the use of nanocrystal floating gates for nonvolatile FLASH memory. Utilizing nanocrystals rather than continuous floating gates for storing charge should allow the use of thinner insulators and improve the scaling potential for future FLASH devices. Recent advances in nanoscale materials and device physics are also behind rapid progress in two other non-volatile memory devices that are entering the commercial arena. Phase Change Memory (PCM) has been in development for decades and is now considered to be a potential successor to silicon FLASH memory because of its superior potential to be scaled to small size. Extensive materials research shows that the phase change behavior is well defined in films as thin as 1 nanometer and exploratory device research suggests that devices with active material volumes of just a few cubic nanometers are feasible. Looking forward advances in the understanding of oxygen vacancy transport in metal oxides and other effects which can induce resistance changes in material stacks may find potential application in other resistive memory devices, including novel “memristor” devices, that may be useful in memory, storage, and even circuits which mimic the synaptic function of the brain. The other emerging non-volatile memory technology is Magnetic Random Access Memory (MRAM). It has been in commercial development since the mid-nineties, and promises much greater speed, lower power, and far better durability than either FLASH memory or PCM. However, a path to very small devices became evident only after a scientific breakthrough the experimental demonstration of the spin-torque transfer effect. See the discussion below of Nanomagnetics and Spintronics. For FETs used in digital logic circuits, the most promising directions forward involve reduced-dimension structures, starting with ultrathin silicon-on-insulator (SOI) and doublegate or Fin-FET devices, ultimately leading to completely 1D structures such as nanowires and nanotubes. All of these structures enable improved gate control of the FET channel current, allowing shorter channels and better performance. Carbon nanotubes (CNTs) in particular have been studied intensely for this over the past 10 years, and many interesting demonstrations have been done that take advantage of their high carrier mobility, high thermal conductivity, and unique physics. The key remaining obstacle to the use of nanotubes and nanowires in high performance electronics is the lack of fabrication methods that allow dense packing of uniform diameter tubes/wires across a large area with low defects and identical electrical behavior. For flexible electronics or applications that currently utilize thin film transistors (TFTs), the requirements are greatly relaxed. Hence the first large-scale application of CNTs may be as a mesh structure for moderate-performance flexible electronics an area of growing importance in the future.

Regardless of the material or structure used, all of the above-mentioned FETs are approaching some hard limits due to the basic physics of the device operation. Thus there is a strong need to explore new device concepts that circumvent these limitations. Similar motivations drove the development of both the first solid state transistors, based on bipolar technology, when vacuum tubes and mechanical switches were reaching similar power constraints in the late 1940s, and the current FET, which replaced bipolar transistors in the majority of semiconductor applica-

 Copyright by AQIE and RIPS

tions in the late 1980s. The potential for yet another major device transition was recognized at the beginning of the decade, and the Semiconductor Research Corporation (SRC) and the National Science Foundation (NSF) jointly organized a set of industry-academia-government workshops to study the problem. In parallel, the Technology Strategy Committee of the Semiconductor Industry Association (SIA) conducted several workshops whose objective was to identify research initiatives to advance integrated circuit technology beyond currently identified scaling limits. These activities ultimately defined key research vectors considered to be important components of the search for the next switch and resulted in the formation of the Nanoelectronics Research Initiative (NRI, http://nri.src.org) by the SIA in 2005. Managed by the SRC, the NRI's mission is to demonstrate novel computing devices capable of replacing the CMOS FET as a logic switch in the 2020 timeframe. These devices must show significant advantage over ultimate FETs in power, performance, density, and/or cost, and most importantly must enable the semiconductor industry to extend the historical cost and performance trends for information technology. The NRI's primary goal is to circumvent the power density issues that are currently limiting CMOS technology. To go beyond this limit, the physics of the device or the mode of its operation must be fundamentally changed so that much less energy is dissipated in each switching operation. To accomplish this, the primary focus is on switches that utilize alternative state variables to represent information (compared to the FET, which relies on the dissipative movement of charge), as well as on the corresponding interconnects and circuits needed to perform logic. Research is also being done on nanoscale phonon engineering, both to manage heat and potentially to isolate systems from thermal noise, and on directed self-assembly of key device structures. The challenge and urgency of finding a new switch to enable continued progress in nanoelectronics beyond 2020, similar to what has driven the economy for the past half century, should not be underestimated and should be one of the primary foci of nanoelectronics work in the coming decade. While many of the nanoelectronic advances in the past decade have already had impact on mainstream electronics, many other breakthroughs show great promise for new innovations in the coming decade. A few examples include:

- The discovery of graphene and development of methods for controlled growth or synthesis
- Elucidation of the electronic, optical and thermal properties of carbon nanotubes and graphene and establishment of a new class of electronic materials – carbon electronics.
- Discovery of magnetoelectric and multiferroic materials which promise voltage-control of magnetism
- The experimental realization of spin torque switching
- Discovery of the Spin Hall Effect
- Demonstrations of spin injection into and spin readout from semiconductors.
- The discovery of topological insulators, a new and topologically distinct electronic state in matter with unique collective transport properties

 Copyright by AQIE and RIPS

- Advances in the understanding and development of dilute magnetic semiconductors
- Fundamental understanding of the chemistry and physics of semiconductor nanowire growth
- . • The exploration of nanoscale solid-state electrochemistry for a variety of potential applications in device technology .
- Some of these breakthroughs have already developed into major new fields of technology exploration, with two of the largest areas currently being graphene electronics and spintronics.

Graphene Electronics

One of the most interesting developments for future nanoelectronics has been the rediscovery of graphene—a single monolayer of graphitic carbon—as a potential substrate with unique physics. This material has almost all of the same advantages of CNTs (as well as other attributes), but it is a planar material, making device fabrication more straightforward. However, producing the initial substrate of graphene is still very challenging. While the electronic structure of graphene was calculated back in 1945, and ways to produce graphene on metals SiC, and graphene oxide were demonstrated early on, research on the electronic properties of graphene did not start earnestly until 2004, when single-layer graphene was exfoliated from graphite and deposited on SiO2. Early experimental and theoretical work was focused on the 2D electron gas properties, particularly on the study of graphene's quantum Hall effect and its minimum conductivity. Transport measurements firmly established its excellent electrical properties: mean-free paths of hundreds of nanometers to a micrometer and mobilities of the order of 10,000 cm2/Vs in the supported state and over 200,000 cm2/Vs in the suspended state. Additionally, graphene possesses extremely high current-carrying capability and excellent thermal conductivity and mechanical strength. Graphene was incorporated early on as the channel of field-effect transistors, and the device current could be modestly modulated by the gate field due to the linear variation of the graphene density-of-states with energy. However, because of the lack of a bandgap (graphene is a zero bandgap semiconductor), the achieved current on/off ratios have been, in general, below 10. Thus, although, graphene was hailed in the popular press as a successor to Si-MOSFETs, the lack of a bandgap currently precludes its use in digital electronics. On the other hand, in bilayer graphene with the layers stacked in the so-called AB or Bernal stacking configuration, the interaction between the two layers was shown theoretically in 2006 to lead to the opening of a bandgap on application of a strong vertical electrical field. Early experiments failed to reveal a significant bandgap opening, most likely because of the quality of the bilayer sample used. In more recent experiments using a better dielectric gate stack, the opening of an electrical bandgap >140 meV was demonstrated, and further improvements are expected. The initial graphene experiments were performed using exfoliated graphite. Soon, however, synthetic techniques for growing monolayer and multilayer graphenes appeared. Currently, the key synthetic techniques involve the thermal decomposition of SiC and chemical vapor deposition on metals such as Ni or Cu. While digital electronic applications are not currently possible for graphene, its ex-

 Copyright by AQIE and RIPS

tremely high carrier mobility at room temperature, ultimate body thinness, high transconductance, and modest field tuning of the current recommend graphene for high-frequency analog electronic applications. In particular, radio-frequency field-effect transistors (RF-FETs) could find use in wireless communications, radar, security and medical imaging, vehicle navigation systems, and a host of other applications. Currently, the record cutoff frequency (fT) achieved by RF graphene transistors based on exfoliated graphite stands at 50 GHz. Of course, for commercial applications, wafer-scale graphene is required. This can be achieved using the above-mentioned graphene synthetic techniques.

In particular, the SiCbased approach has yielded wafer-sized samples of graphene. Graphene wafers from the Siface of SiC show good layer thickness control and morphology and have mobilities that currently are in the range of 1,000 to 3,000 cm2/Vs. C-face SiC yields graphene with higher mobilities but with thicker layers and less controlled morphology. RF transistors have been fabricated on Si-face SiC-derived 2-inch graphene wafers. The current record involves 240 nm gate length transistors from IBM with cutoff frequencies of 100 GHz . This is already remarkable since Si-CMOS transistors with the same gate length achieve cutoff frequencies of 40 GHz. The currently achieved fT x (gate length) product of 22 GHz · μm is higher than that of most semiconductors, and both scaling of the devices and improvements in the graphene mobility are expected to yield much higher-frequency performance. Another possible area for applications of graphene that can utilize its exceptional transport properties for both electrons and holes, as well as its strong optical absorption over a very wide wavelength range (about 2% per atomic layer), is optoelectronics. Ultrafast (>40 GHz) metal-graphene-metal photodetectors have been demonstrated, and these photodetectors have been used recently to detect reliably optical data streams at 10 Gbits/s. THz radiation emitters from monolayer and bilayer graphene are also very likely to emerge soon. Finally, beyond the traditional electron transport and optical devices, the physics of graphene could offer new possibilities for devices with unique functionality. The two-dimensional honeycomb lattice of graphene gives rise to a conical band structure, which leads to electrons behaving as massless Dirac fermions. Some proposed devices take advantage of the resulting photon-like behavior of electrons in graphene and utilize p-n junctions to create programmable interconnects or Veselago lens devices.

A completely different approach is taken by another new transistor concept, the bilayer pseudospin FET (BiSFET). In this device, two metal oxide gates sandwich two separately contacted graphene monolayers separated by a tunnel oxide. This device takes advantage of the pseudospin property, which predicts that under certain gate conditions an exciton condensate forms between the graphene layers, leading to the possibility of a collective many-body current between the two layers.This could potentially enable a very low-energy switch, even at room temperature (A) Scanning electron microscope image and the schematic cross-sectional view of a top-gated graphene field-effect transistor. The optical image of the two-inch grapheme /SiC wafer with arrays of graphene devices is on the right. The transistors possess dual-gate channels to increase the drive current and lower the gate resistance. The

 Copyright by AQIE and RIPS

scale bar is 2 μm. (B) Drain current ID of a 240- nm gate length graphene transistor as a function of gate voltage VG at drain bias of 1 V. The current shown was normalized with respect to the total channel width. The device conductance gm = dID/dVG is shown on the right axis. (C) Measured drain current ID as a function of drain bias of a graphene FET with a gate length Lg of 240 nm for various top-gate voltages. (D) Measured small signal current gain ∣h21∣ as a function of frequency f for a 240-nm gate), respectively.ρ) and (↓and a 550-nm gate graphene FET, represented by (The current gain for both devices exhibits 1/f dependence, where a welldefined cutoff frequency fT can be determined to be 53 GHz and 100 GHz for the 550-nm and 240-nm devices, respectively.

Nanomagnetics and Spintronics

While electronics and semiconductors have traditionally formed the basis for the chip industry, magnetics has formed the basis for the storage industry. During the past 10 years, though, advances in nanometer-sized magnetic devices as well as new methods for controlling spin properties in general have enabled increased usage of nanomagnetics, including on chip. There have been significant advances in spintronics, particularly in areas based on a nanoscale multilayer structure, that is, a magnetic tunnel junction (MTJ). Magnetic tunnel junctions are already ubiquitous in that they are the key component in the sensor that reads the information stored on a magnetic disk. In 2006, a new type of nonvolatile, infinite-endurance computer memory was introduced to the marketplace called magnetic random access memory or MRAM. This memory is now manufactured and sold by a spinoff of Freescale Semiconductor called Everspin, which has been introducing MRAM into more and more markets over the last few years. MRAM is also going to be a key component in defense systems that require radiation-hard, nonvolatile memory; Honeywell has teamed with Everspin to provide just such a product that is now going into production. The MTJ can also be used as a sensor, and this has found several applications in industrial sensing as well as in cell phones to provide directional information (a 3D magnetic compass). Several key discoveries led to the successful development of MRAM, including a novel method of switching the bit, called toggle-switching, and the discovery of a new tunnel barrier (MgO) that enabled an order-of-magnitude increase in the tunneling magnetoresistive ratio (TMR).

In the beginning of the last decade, another major hurdle for MRAM was overcome with the discovery of magnetization reversal due to scattering of a spin-polarized current. This discovery, called spin torque transfer (ST or STT) switching, will allow MRAM to scale to well under 10 nanometers, dimensions that traditional switching methods using current-generated magnetic fields will never allow. Spin torque transfer also enables the generation of spin wave radiation due to the rapidly precessing magnetization of the “free layer” of a tunnel junction in a magnetic field. These nano-oscillators may find many uses in signal generation and processing as well as in phased arrays for RF detection and radiation. Finally, spin torque transfer provides a means to move magnetic domain walls in a magnetic nanowire.. This provides an alternate path for information storage and perhaps even processing. Prior to the discovery of spin torque transfer, magnetic domain walls were moved

 ∣ Copyright by AQIE and RIPS

using changing magnetic fields, which are cumbersome and power-hungry. Another major direction for spintronics was enabled by the realization that traditional semiconductors could be made magnetic by adding dilute amounts of magnetic ions, particularly manganese .These materials, by virtue of the fact that in most cases the magnetism is mediated by carriers and carrier concentrations can be controlled electrically offer the unprecedented ability for the magnetism to be controlled with an electric field. The field of semiconductor spintronics has grown exponentially in the last decade but has been hindered by the absence of a magnetic semiconductor with a Curie temperature well above room temperature. However, proof of principle demonstrations of various spin-injection and FET-like devices show that if the right material is found, then adding the spin degree of freedom to semiconducting devices will enable a broad spectrum of applications spanning many diverse fields of electronics and photonics.

 | Copyright by AQIE and RIPS